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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,853	09/05/2003	Gregory Starr	ALT-255	7257

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EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,853	STARR, GREGORY	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,7,8,18-23,27,28 and 30-43* is/are rejected.

7)☒ Claim(s) *4-6,9-17,24-26 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12-16-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's Amendment filed on 6-2-05 has been received and entered in the case. The rejections set forth in the previous Office Action are maintained in a revised form to accommodate amendment of claims as indicated below.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 3, 7, 8, 18, 21-23, 27, 28, 30-32, 34, 37 and 42-43 are rejected under 35 U.S.C. 102(b) as being anticipated by the Riley, Jr. reference (U.S. Patent 4,272,729).

Riley discloses in figure 1 an PLL circuit having an input terminal for receiving a reference signal fREF and an output terminal for outputting an output signal fOUT locked to said reference signal, and comprising a compensation component 12 for producing said output signal; a high-gain coarse feedback path 34 feeding said compensation component, said high-gain coarse feedback path accepting as inputs said reference signal and said output signal, and causing said compensation component to drive said output signal to within a predetermined variance from said reference signal (function of PLL circuit); wherein the coarse feedback path comprises a frequency detector 26 having inputs connected to said input terminal and said output terminal via divider 16, the frequency detector producing a coarse-adjust signal 28 based on difference between the output frequency and the reference frequency, and a high-gain signal modifier 30 downstream of the frequency detector; and a low-gain fine feedback path 44 feeding said

compensation component, said low-gain fine feedback path accepting as inputs said reference signal and said output signal, and causing said compensation component to drive said output to a lock with said reference signal after said coarse feedback path has caused said compensation component to drive said output signal to within said predetermined variance from said reference signal (See abstract) wherein the fine feedback path comprising a phase-frequency detector 18 having inputs connected to the input terminal and the output terminal, the phase-frequency detector producing a fine-adjust signal (output of 18) based on the difference between said output frequency and the reference frequency, and a low-gain signal modifier 44 downstream of the phase-frequency detector as required by claim 3.

As to claim 7, Riley discloses a control circuit 44 adapted to disable said fine feedback path until said coarse feedback path is locked and to enable said fine feedback path after said coarse feedback path is locked.

As to claim 8, figure 1 discloses the frequency detector 18 (see column 8, lines 19-22) is programmable by means of programmable divider 16.

As to claim 18, Riley discloses the fine feedback path comprising a charge pump 20 and a loop filter 22 between the phase-frequency detector and the low-gain signal modifier.

As to claim 21, Riley discloses a feedback scaling counter 16 between the output terminal and each said feedback path.

As to claim 22, the scope of claim is similar to that of claim 2. Therefore, it is rejected for the same reason set forth above. It is noted that PLL and DLL circuits, in general, is used interchangeably.

As to claim 23, figure 1 of Riley discloses said coarse feedback path comprising a first phase detector 26 (see col. 3, lines 19-23) having inputs connected to said input terminal and said output terminal, said first phase detector producing a coarse-adjust signal 28 based on difference between said output phase and said input phase, and a high-gain signal modifier 32 downstream of said phase detector; and said fine feedback path comprising a second phase detector 18 having inputs connected to said input terminal and said output terminal, said second phase detector producing a fine-adjust signal (output of 18) based on difference between said output phase and said input phase, and a low-gain signal modifier 22 downstream of said second phase detector.

As to claim 27, the scope of claim is similar to that of claim 7. Therefore, it is rejected for the same reason set forth above.

As to claim 28, the scope of claim is similar to that of claim 8. Therefore, it is rejected for the same reason set forth above.

As to claim 30, the scope of claim is similar to that of claim 18. Therefore, it is rejected for the same reason set forth above.

As to claim 31, figure 1 of Riley discloses the predetermined variance is programmable by FRE. DATA signal.

As to claim 32, column 13, lines 51-53, discloses the claimed invention.

As to claim 34, it is inherent that an integrated circuit is commonly mounted on a circuit board.

As to claim 37, the scope of claim is similar to that of claim 32. Therefore, it is rejected for the same reason set forth above.

As to claim 42, the PLL of Riley comprises a programmable divider 16. Therefore, the limitation "the predetermined variance is programmable" is anticipated by the Riley reference.

As to claim 43, the scope of claim is the same as that of claim 22. Therefore, it is rejected for the same reason set forth above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Riley Jr. reference (U.S. Patent 4,272,729) in view of the Berry et al reference (U.S. Patent 6,366,174).

Riley discloses all the claimed invention except for teaching an output scaling counter downstream of the output terminal and an input scaling counter upstream of the input terminal as required by claims 19 and 20.

Berry et al discloses in figure 1 a PLL circuit comprising, among other things, an output scaling counter 44 downstream of the output terminal 42 and an input scaling counter 22 upstream of the input terminal (20) as required by the claims.

It would have been obvious to one skilled in the art at the time invention for one skilled in the art to incorporate the teachings of Berry into that of Riley for the purpose of adjusting frequency of signal. A skilled artisan in the art would have been motivated to combine the above

teachings to achieve a proper frequency/phase of signal which is suitable for further processing downstream of the circuit as required by a particular application.

5. Claims 33, 35, 36, 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Jefferson reference (U.S. Patent 5,744,991) in view of the Riley Jr. reference (U.S. Patent 4,272,729).

Jefferson discloses in figure 2 an apparatus comprising a processing circuit 101A ; a memory 105A coupled to the processing circuit; and a PLL circuit 121A coupled to the processing circuit and the memory as partially required by claim 33. Jefferson does not disclose a PLL circuit comprising elements being configured as required claim. It is noted that Jefferson circuit is an ICs mounted on a printed circuit board (col. 1, lines 5-20).

Riley discloses a PLL circuit that is required by claim as noted above.

It would have been obvious to one skilled in the art at the time the invention was made to incorporate the PLL circuit taught by Riley into that of Jefferson since a PLL circuit is known to be implemented in many different ways.

A skilled artisan would have been motivated to use the PLL circuit taught Riley since Riley's PLL circuit would insure a phase lock-up when factors such as misalignment of the oscillator, aging of components and/or temperature are presented.

As to claims 35 and 36, the scopes of claims are similar to the combination scope of claims 33 and 34. Therefore, they are rejected for the same reasons set forth above.

As to claims 38-41, the scopes of claims are similar to that of claims 32-35. Therefore, they are rejected for the same reasons set forth above.

Response to Arguments

6. Applicant's arguments filed 11-8-04 have been fully considered but they are not persuasive.

As to the rejections of claim 10 under 35 USC 102(b) by the Riley reference, Applicant has argued that Riley the phase detector 18 of Riley does not produce a fine-adjust signal based on the difference between an output frequency and a reference frequency. Examiner respectfully disagrees since the output frequency fOUT is provided to the phase detector 18 via divider 16. Further, there is no drawing of the instant application showing a direct coupling of the output frequency to the phase/frequency detector.

As to the rejections of claim 22 under 35 USC 102(b) by the Riley reference, Applicant has argued that PLL and DLL circuits are not interchangeable. Examiner respectfully disagrees since it is well known in the art that PLL and DLL circuits are nearly identical, structurally and operationally (i.e., arrangement of phase/fre. detector and VCO for synchronizing signals). A phase locked loop (PLL) arrangement is called a delay locked loop (DLL) when the phase of a fixed-frequency oscillator is shifted directly is. For further information, see US Patents 6,323,910 or 6,909,317.

Allowable Subject Matter

7. Claims 4-6, 9-17, 24-26 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus comprising elements being configured as recited in claim. Specifically, none of the prior art teaches or fairly suggests, among other things, the following limitations:

- Said oscillator is a current-controlled oscillator; said low-gain signal modifier is a voltage-to-current converter having a first gain; and said high-gain signal modifier is a voltage-to-current converter having a second gain greater than said first gain as required by claims 4 and 24.
- Each of said high-gain signal modifier and said low-gain signal modifier has a respective gain; and said gain of said high-gain signal modifier is ten times said gain of said low-gain signal modifier as required by claims 6 and 26.
- A specific configuration of the frequency detector as recited in claim 9.
- A coarse feedback path further comprises a digital-to-analog converter between said phase detector and said high-gain modifier as required by claim 29.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
6-23-05

TIMOTHY P. CALLAHAN
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